Appl. No. 10/738,472
Examiner: Warren, Matthew E., Art Unit 2815
In response to the Office Action dated January 25, 2005

Date: April 25, 2005
Attorney Docket No. 10113491

REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority and receipt of the certified copy of the priority document. Responsive to the Office Action mailed on January 25, 2005 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-47 are pending. Claims 1-16 are withdrawn from consideration. Claims 28-47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter with which Applicant regards as the invention. Claims 17-19, 25, 26 and 28-32 are rejected under 35 U.S.C. 103(a) as being anticipated by Hsiao et al (US 6,391,705) in view of Gruening et al (US 6,184,09). Claims 20-24 and 27 are rejected under 35 U.S.C. 103(a) as being anticipated by Hsiao et al in view of Gruening et al and further in view of Nitayama et al (US 6,720,606). Claims 33-35, 41, 42 and 44-47 are rejected under 35 U.S.C. 103(a) as being anticipated over Hsiao et al in view of Jammy et al (US 6,222,218) and Gruening et al. Claims 36-40 and 43 are rejected under 35 U.S.C. 103(a) as being anticipated over Hsiao et al in view of Jammy et al and Gruening et al and further in view of Nitayama et al.

In this paper, claims 28 and 33 are amended to overcome the rejections under 35 U.S.C. 112. Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Rejections Under 35 U.S.C. 112

Claims 28-47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter with which Applicant regards as the invention.

Claim 28 has been amended to recite the conducting wire has a first conducting layer and a second conducting layer, ***the first conducting layer of*** the conducting wire and the substrate

are isolated by a circular insulating layer, and the second conducting layer ***lies on*** the first conducting layer and the circular insulating layer. Support for this amendment can be found on page 5, lines 19-29 and Fig. 2 of the application. Applicant submits that the rejections of claims 28-32 under 35 U.S.C. 112 are thereby overcome.

Claims 33 has been amended to recite etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating layer to leave a remaining first insulating layer on a sidewall of the second insulating layer, in which a trench top insulating layer consists of the first remaining insulating layer and the second insulating layer. Support for this amendment can be found on page 6, lines 3-25 and Fig. 3 of the application. Applicant submits that the rejections of claims 33-47 under 35 U.S.C. 112 are thereby overcome.

Rejections Under 35 U.S.C. 103(a)

Claims 17-19, 25, 26 and 28-32 are rejected under 35 U.S.C. 103(a) as being anticipated by Hsiao et al in view of Gruening et al. Claims 20-24 and 27 are rejected under 35 U.S.C. 103(a) as being anticipated by Hsiao et al in view of Gruening et al and further in view of Nitayama et al. Claims 33-35, 41, 42 and 44-47 are rejected under 35 U.S.C. 103(a) as being anticipated over Hsiao et al in view of Jammy et al and Gruening et al. Claims 36-40 and 43 are rejected under 35 U.S.C. 103(a) as being anticipated over Hsiao et al in view of Jammy et al and Gruening et al and further in view of Nitayama et al. Applicant respectfully traverses the rejections for the reasons as follow.

Hsiao et al teach a fabrication method of a high-density semiconductor memory cell structure having a trench. In Hsiao et al, a trench top isolation layer 802 consists of a single insulation layer. Gruening et al teach the formation of a controlled trench top-isolation layer for vertical transistors. In Gruening et al, trench top isolation layer 44 consists of a single insulation layer formed from SACVD layer 40. Jammy et al and Nitayama et al teach the formation of a DRAM trench and dynamic semiconductor memory device, respectively.

None of the cited references, whether taken alone or in combination, teach or suggest a method for fabricating a memory device with a vertical transistor and a trench capacitor comprising the step of forming a trench top insulating layer on a conducting wire, in which the trench top

insulating layer consists of a first insulating layer and a second insulating layer surrounded by the first insulating layer, as recited in claim 17.

MPEP 2142 reads in part:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

In the rejection of claim 17, the Examiner relies upon Gruening et al to teach a method of forming a memory device comprising the step of forming "a top insulating layer (40 in fig. 3) having a first insulating layer (36) and a second insulating layer (44) surrounded by the first insulating layer." See page 4 of the office action.

However, in Gruening et al, nitride liner 36 is not a part of the trench top isolation layer. Namely, Gruening et al clearly refers to "trench top isolation layer 44", which is a ***single*** insulation layer formed from SACVD layer 40. See column 5, lines 18-19 and 46-47, column 6, lines 13-21, and Figs. 3-5.

In Gruening et al, nitride layer 36 is stripped from trench sidewall, preferably by a wet etching process. See column 5, lines 54-57 and Fig. 5 of Gruening et al. Thus, nitride layer 36 is only a temporary element utilized in the deposition of the SACVD layer 40 and then later ***removed in its entirety***. Its therefore follows that nitride layer 36 is not a part of the "trench top isolation layer" or "memory device" described in Gruening et al's teaching.

Applicant therefore submits that even when combined, the cited references fail to teach or suggest a method for fabricating a memory device with a vertical transistor and a trench capacitor comprising the step of forming a trench top insulating layer on a conducting wire, in which ***the trench top insulating layer consists of a first insulating layer and a second insulating layer surrounded by the first insulating layer***, as recited in claim 17.

For at least this reason, it is Applicant's belief that claim 17 is allowable over the cited references. Insofar as claims 18-32 depend from claim 17, it is Applicant's belief that these claims are also in condition at least by virtue of their dependency from claim 1. The Examiner's arguments in connection with claims 2-17 are therefore considered moot and will not be addressed here.

The office action fails to establish some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine Hsiao et al and Gruening et al in the manner relied upon in the rejections of claims 17-32.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

With respect to Gruening et al's use of a temporary nitride layer 36 in the formation of SACVD layer 40, the office action states on page 4:

> Gruening et al discloses a method of forming a memory device comprising the step of forming a top insulating layer (40 in fig. 3) having a first insulating layer (36) and a second insulating layer (44) surrounded by the first insulating layer. With such a

configuration, an improved trench top isolation is formed (column 5, lines 13-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trench top oxide of Hsiao by using a first and second insulating layer as taught by Gruening to form an improved, reliable trench top insulation.

However, as noted above, layer 40 is an SACVD layer. The "improved trench top isolation layer 44" referred to in column 5, lines 18-19 of Gruening et al refers to a ***single*** insulation layer formed from SACVD layer 40, and does not refer to nitride layer 36 in any way. In Gruening et al, the purpose of nitride layer 36 is to form a SACVD layer with a thicker bottom and thinner sidewall according to different growth rates on silicon and nitride. See column 5, lines 4-7. While nitride layer 36 is utilized in the deposition of the SACVD layer 40, it is later ***removed in its entirety*** and does not make up a part of the "improved trench top isolation layer 44" taught in Gruening et al. This teaching does not support the motivation relied upon by the Examiner.

Indeed, as Gruening et al do not even teach a trench top isolation layer having a first insulating and a second insulating layer surrounded by the first insulating layer, it is Applicant's belief that the combined teachings of Gruening et al and Hsiao et al provide no suggestion or motivation to one of ordinary skill in the art to employ a trench top isolation layer having a first insulating and a second insulating layer surrounded by the first insulating layer in Hsiao et al's structure. The only suggestion or motivation to make the combination relied upon by the Examiner appears to come from Applicant's own disclosure.

For at least this reason, it is Applicant's belief that rejections of claims 17-32 should be withdrawn and the claims passed to issue.

None of the cited references, whether taken alone or in combination, teach or suggest a method for fabricating a memory device with a vertical transistor and a trench capacitor comprising the step of etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating layer to leave a remaining first insulating layer on a sidewall of the second insulating layer, in which a trench top insulating layer consists of the remaining first insulating layer and the second insulating layer, as recited in claim 33.

For the same reasons discussed in connection with claim 17, it is Applicant's belief that, even when combined, the cited references fail to teach or suggest the formation a memory device including the step of forming a trench top insulating layer consisting of the first remaining insulating layer and the second insulating layer.

In addition, the Examiner asserts that Hsiao et al teach filling a second insulating layer (802) in the deep trench. Applicant respectfully disagrees this assertion. On the contrary, Hsiao et al teach that the insulating layer (802) is formed by thermal oxidizing a poly silicon layer. See column 4, lines 44-46.

Furthermore, the Examiner asserts that Gruening et al teach etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating layer to leave the remaining first insulating layer on a sidewall of the second insulating layer, in which a trench top insulating layer consists of the first insulating layer and the second insulating layer. However, in Gruening et al, nitride layer 36 is removed in its entirely. See column 5, lines 54-55 of Gruening et al. Nitride layer 36 is not etched to leave a remaining portion that is part of the trench top isolation layer. Hsiao also fails to teach this limitation. See column 4, lines 57-59 of Hsiao et al.

For at least these reasons, it is Applicant's belief that claim 33 is allowable over the cited references. Insofar as claims 34-47 depend from claim 33, it is Applicant's belief that these claims are also in condition at least by virtue of their dependency from claim 33. The Examiner's arguments in connection with claims 34-47 are therefore considered moot and will not be addressed here.

<u>The office action fails to establish some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine Hsiao et al and Gruening et al in the manner relied upon in the rejections of claims 33-47.</u>

In connection with the rejection of claim 33, the Examiner states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trench top oxide of Hsiao et al by using a first and second insulating layer as taught by Gruening et al to form an improved, reliable trench top insulation. See page 8 of the office action. For the same

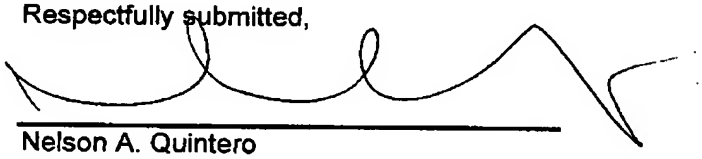
reasons stated in connection with claim 17, it is Applicant's belief that the combined teachings of Gruening et al and Hsiao et al provide no suggestion or motivation to one of ordinary skill in the art to employ a trench top isolation layer consisting of the remaining first insulating layer and the second insulating layer in Hsiao et al's structure.

For at least this reason, it is Applicant's belief that rejections of claims 33-47 should be withdrawn and the claims passed to issue.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



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